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J1059 U.S. PTO

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Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

New U.S. Patent Application
Title: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
AND THE SEMICONDUCTOR DEVICE
Inventors' Names and Addresses:

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Sir:

We enclose the following papers for filing in the United States Patent and Trademark Office in connection with the above patent application.

1. Application- 24 pages, including 6 independent claims and 14 claims total.

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October 11, 2001

Page 2

2. Drawings- 20 sheets of formal drawings containing 38 figures.
3. Certified copy of Japanese Application No. 2000-312015, filed October 12, 2000.
4. Information Disclosure Statement and Information Disclosure Citation, PTO 1449 with 1 document attached.
5. The filing fee is calculated as follows:

Basic Application Filing Fee					\$740	\$ \$740.00
	Number of Claims		Basic	Extra Claims		
Total Claims	14	-	20		x \$18	
Independent Claims	6	-	3	3	x \$84	252.00
<input type="checkbox"/> Presentation of Multiple Dep. Claim(s)					+\$280	
Subtotal						\$ 992.00
Reduction by 1/2 if small entity						-
TOTAL APPLICATION FILING FEE						\$ 992.00

6. A check for \$992.00 is enclosed. The fee includes:

\$740.00 filing fee; and
\$252.00 additional claims fee

This application is being filed under the provisions of 37 C.F.R. § 1.53(f). Applicants await notification from the Patent and Trademark Office of the time set for filing the Declaration.

Applicants claim the right to priority based on Japanese Application No. 2000-312015, filed October 12, 2000.

Please address all correspondence with respect to this application to:

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October 11, 2001
Page 3

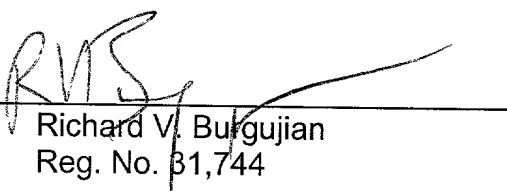
Please accord this application an application number and filing date.

The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16 or §1.17 during the pendency of this application to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By:


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Reg. No. 31,744

RVB/FPD/gah
Enclosures

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